REMARKS

This is a full response to the outstanding FINAL Office Action mailed November 26, 2007 and the ensuing Advisory Action mailed March 20, 2008. The Examiner is thanked for the thorough examination of the present application. In the Advisory Action, the Examiner indicates that the amendments made in the response to FINAL Office Action have been entered. The Examiner, however, maintains the rejection of the claims. In response to the Examiner's comments set forth in the Advisory Action, Applicants have amended some of the claims in an effort to advance prosecution and respectfully request consideration of the following remarks contained herein.

I. Response to Claim Rejections Under 35 U.S.C. §101

Claims 1-6, 13-16, 20-24, and 32-35 remain rejected under 35 U.S.C. §101 because the claimed invention is allegedly directed to non-statutory subject matter. In particular, the Advisory Action alleges that the various claims do not clearly or directly provide "*a practical/physical application of the algorithm*" to determine the minimum or maximum value. (Advisory Action, Continuation sheet, page 2). Applicants respectfully submit that claims 1, 17, 20, and 36 are directed to structural features (*e.g.*, a processor, customer premises equipment), which are clearly directed to more than just an algorithm or an abstract idea. With regards to claims 13 and 32, which are directed to process claims, Applicants have amended these claims to recite a useful, concrete, and tangible result. Based on the foregoing, Applicants respectfully request that the §101 rejection be withdrawn.

II. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102. Claims 1-6, 13-15, 20-24, and 32-34 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Okumura et al. (U.S. Pat. No. 5,726,923, hereinafter "Okumura"). For at least the reasons set forth below, Applicants respectfully traverse these rejections.

Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 1.

Claim 1 recites (emphasis added):

> 1. A processor for reducing the processing effort for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the processor comprising:
> a destination register;
> a first source register storing a first value, wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register;
> a second source register storing a second value, wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register;
> means for comparing the first value stored in the first source register with the second value stored in the second source register;
> ***means for storing the first value in the destination register when the first value is less than or equal to the second value***; and

> means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value.

In the Advisory Action, Examiner addresses Applicants' arguments regarding the feature, "means for storing the first value in the destination register when the first value is less than or equal to the second value." In asserting that Applicants' arguments are unpersuasive, the Examiner states that Applicants have "*applied the incorrect path for this limitation*" (in reference to storing the first value in the destination register when the first value is less than or equal to the second value). The Examiner further states that "*the correct path is to execute S9 when the register 5 is less than specific register 11. This path would clearly meet the argued feature above*." (Continuation Sheet, page 2).

Applicants are somewhat puzzled by the Examiner's reference to "the correct path" as the claim language clearly addresses both conditions – 1) when the first value is less than or equal to the second value; and 2) when the second value is less than the first value. In particular, claim 1 clearly recites means for performing certain steps for both conditions. With reference to the Okumura reference, the Examiner makes the following correlations:

> "first source register" in claim 1: "specific register 11" in Okumura
> "second source register" in claim 1: registers 5-6 in Okumura
> "destination register" in claim 1: "specific register 11" in Okumura

(*See* FINAL Office Action mailed November 26, 2007, page 3.) If the content of register 5 (allegedly the "second source register" in claim 1) is judged to be less than the content of the specific register 11 (allegedly the "first source register" in claim 1), step s9 is executed. In step S9, the content of register 6 and the counted result of the

counter 9 are "linked" in the index linking circuit 10, and the linked result is stored in the specific register 11. At most, this correlates with "means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value."

Okumura, however, fails to teach of storing the first value in the destination register when the first value *is less than or equal* to the second value. Reference is made to the related text for steps S7-S9 in FIG. 3 of Okumura. If the content of register 5 (allegedly the "second source register" in claim 1) is judged to be larger than or equal to the content of the specific register 11 (allegedly the "first source register" in claim 1), Okumura only teaches that step s9 is not executed. Okumura does not teach of storing the first value (specific register 11) in the destination register (specific register 11) when the first value (specific register 11) is less than or equal to the second value (registers 5-6). Claim 1 explicitly recites means for performing a certain function depending on the relationship between the first value and the second value, while Okumura doesn't appear to address this in the cited text/figure. In this respect, Okumura fails to teach of (means for) "storing the first value in the destination register when the first value is less than or equal to the second value."

Based on the foregoing, Applicants respectfully submit that independent claim 1 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 1 above. Furthermore, Applicants submit that dependent claims 2-6 are allowable for at least the reason that these claims

depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 13

Applicants respectfully submit that independent claim 13 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 13.

Claim 13, as amended, recites (emphasis added):

> 13. A method for reducing a number of processor cycles for determining a minimum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:
> for each of the plurality of source registers,
> comparing a value stored in the source register with a value stored in a destination register;
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register; and
> ***wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers***.

In addressing Applicants' arguments in the Advisory Action, the Examiner continues to reason that since claim 13 does not specify any particular value for "an index value" and "a value of a first source register", these two values are arbitrary. While claim 13 does not specify particular values for the index value and the value of the first source register, Applicants emphasize that the destination register is not initially set to an arbitrary value. Okumura teaches of assigning the value 0x7FFF because this represents the maximum value of the numeric data ("the initial value is preferably

the maximum value within the expressible scope of the numeric data" -- col. 1, lines 57-59). Okumura fails to teach or suggest that the destination register initially includes an index value and a value of a first source register of the plurality of source registers.

Accordingly, Applicants respectfully submit that independent claim 13 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 13 above. Furthermore, Applicants submit that dependent claims 14-16 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 20

Applicants respectfully submit that independent claim 20 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 20.

Claim 20, as amended, recites (emphasis added):

> 20. A processor for determining a maximum value of a plurality of values stored in source registers and determining an index value of a source register having the maximum value, the processor comprising:
> a destination register;
> a first source register storing a first value;
> a second source register storing a second value;
> means for comparing the first value stored in the first source register with the second value stored in the second source register, ***wherein the first source register and the second source register both include a status bit to indicate whether the respective register is active or inactive,*** and wherein a value of a register having an active status is greater than a value of a register having an inactive status;
> means for storing the first value in the destination register when the first value is greater than or equal to the second value; and

means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is greater than the first value.

Applicants have amended claim 20 and submit that no new matter is added by the amendment. Applicants submit that the Okumura reference fails to teach the limitation, "wherein the first source register and the second source register both include a status bit to indicate whether the respective register is active or inactive." That is, Okumura fails to disclose, teach, or suggest the existence of a status bit for indicating the status of a given register. Applicants respectfully submit that the absence of the index field is not equivalent to a status bit that indicates the status of a register. The Examiner relies on the existence (and absence) of the index field in the Okumura reference to anticipate the status bit recited in claim 20. Claim 20, however, has been amended to include a "status bit to indicate whether the respective register is active or inactive." The Okumura reference fails to disclose, teach, or suggest this feature.

Based on the foregoing, Applicants respectfully submits that Okumura fails to teach the feature emphasized above in claim 20. Furthermore, Applicants submit that dependent claims 21-24 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 32

Applicants respectfully submit that independent claim 32 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 32.

Claim 32 recites (emphasis added):

32. A method for reducing the processing effort for determining a maximum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:

for each of the plurality of source registers,

comparing a value stored in the source register with a value stored in a destination register;

concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is greater than the value stored in the destination register; and

wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers.

In addressing Applicants' arguments in the Advisory Action, the Examiner continues to reason that since claim 32 does not specify any particular value for "an index value" and "a value of a first source register", these two values are arbitrary. While claim 13 does not specify particular values for the index value and the value of the first source register, Applicants emphasize that the destination register is not initially set to an arbitrary value. Okumura teaches of assigning the value 0x7FFF because this represents the maximum value of the numeric data ("the initial value is preferably the maximum value within the expressible scope of the numeric data" -- col. 1, lines 57-59). Okumura fails to teach or suggest that the destination register initially includes an index value and a value of a first source register of the plurality of source registers.

Accordingly, Applicants respectfully submit that independent claim 32 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 32 above. Furthermore, Applicants submit that dependent claims 33-35 are allowable for at least the reason that these claims depend from an allowable independent claim.

III. Response to Claim Rejections Under 35 U.S.C. § 103

The USPTO has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP §2141, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

Claims 16-19 and 35-38 remain rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Okumura. For at least the reasons set forth below, Applicants traverse the §103 rejections set forth in the Office Action.

Independent Claim 17

Applicants respectfully submit that independent claim 17 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 17.

Claim 17 recites (emphasis added):

> 17. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:

compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;

store the first value in a first destination register of the processor when the first value is less than or equal to the second value; and

store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value, the index value representing the second source register.

In the Advisory Action, the Examiner continues to assert that FIG. 2 of Okumura "*clearly discloses the numeric field and the index field"* and further asserts that "*the result of the comparison is saved/stored in the numeric data field called the first destination register. . .*" At most, this corresponds with the feature of storing the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value.

Applicants submit, however, that Okumura fails to disclose a processor adapted to store the first value in a first destination register of the processor when the first value is greater than or equal to the second value. Based on a comparison between the first value and second value, the processor performs a certain action. If the first value is less than or equal to the second value, the processor stores the first value in a first destination value. If the second value is less than the first value, the processor stores the second value in the first destination register of the processor and an index value in a second destination register. Okumura at most discloses the latter feature but fails to disclose a processor adapted to store the first value in a first destination register of the processor when the first value is less than or equal to the second value. The Examiner relies on FIG. 3 of Okumura to teach these features.

According to FIG. 3, step s9 is performed if register 5 is less than specific register 11. However, when specific register 11 is less than register 5, then Okumura only discloses that step s9 is not executed. (*See* related text for FIG. 3, Okumura.) Okumura fails to disclose a processor adapted to take action under both conditions.

Accordingly, Applicants respectfully submit that independent claim 17 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 17 above. Furthermore, Applicants submit that dependent claims 18-19 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 36

Applicants respectfully submit that independent claim 36 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 36.

Claim 36 recites (emphasis added):

> 36. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;
> ***store the first value in a first destination register of the processor when the first value is greater than or equal to the second value; and***
> store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater

than the first value, the index value representing the second source register.

In the Advisory Action, the Examiner relies on the same reasoning used to reject claim 17 to reject claim 36. Specifically, the Examiner continues to assert that FIG. 2 of Okumura "*clearly discloses the numeric field and the index field*" and further asserts that "*the result of the comparison is saved/stored in the numeric data field called the first destination register*. . ." This at most corresponds with the feature of storing the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value, the index value representing the second source register.

Applicants submit, however, that Okumura fails to disclose a processor adapted to store the first value in a first destination register of the processor when the first value is greater than or equal to the second value. Based on a comparison between the first value and second value, the processor performs a certain action. The processor is adapted to 1) store the first value in a first destination register of the processor when the first value is greater than or equal to the second value; and 2) store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value, the index value representing the second source register. Okumura at most discloses a processor adapted to handle one of these conditions. The Examiner relies on FIG. 3 of Okumura to teach these features. According to FIG. 3, step s9 is performed if register 5 is greater than specific register 11. However, when specific register 11 is greater than register 5, then step s9 is not executed. (*See* related text for FIG. 3, Okumura.) Okumura fails to disclose a processor adapted to take action under

both conditions.

Accordingly, Applicants respectfully submit that independent claim 36 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 36 above. Furthermore, Applicants submit that dependent claims 37-38 are allowable for at least the reason that these claims depend from an allowable independent claim.

IV. Conclusion

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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